

FIG. 1A

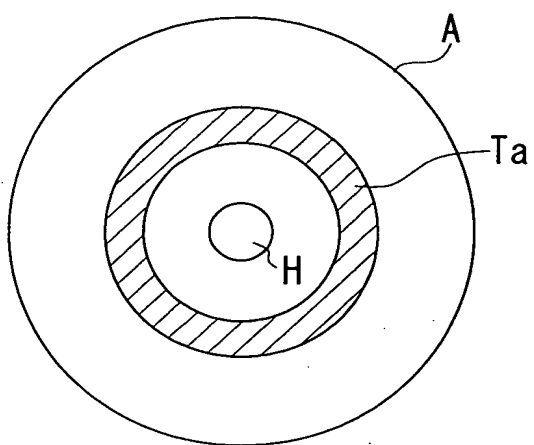


FIG. 1C

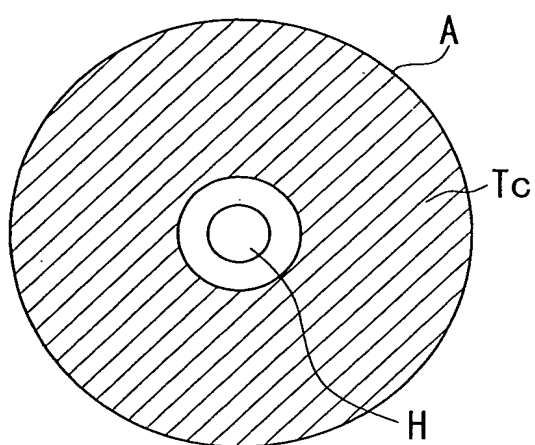


FIG. 1B

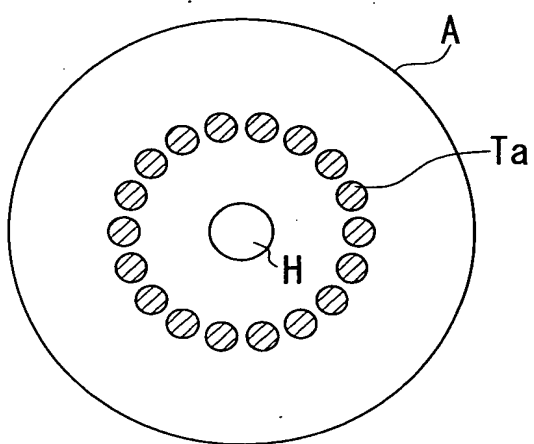


FIG. 1D

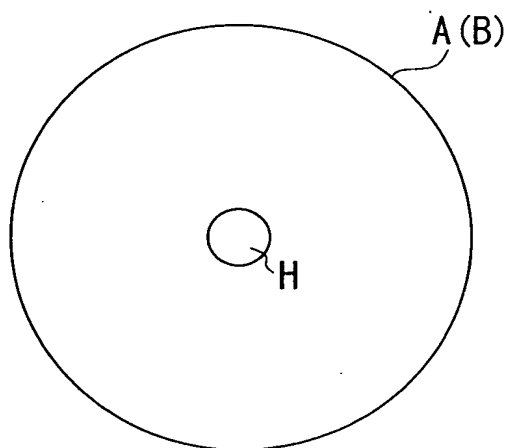


FIG. 2

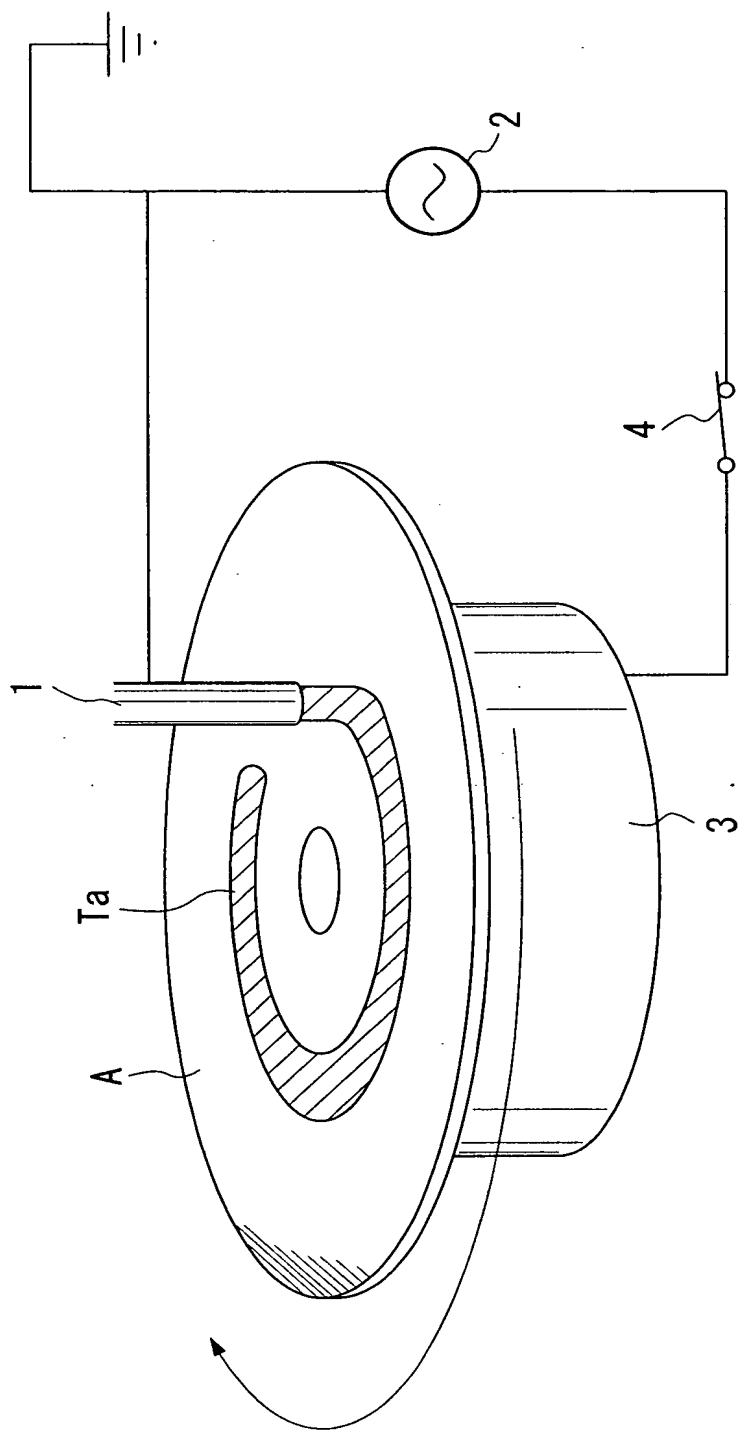
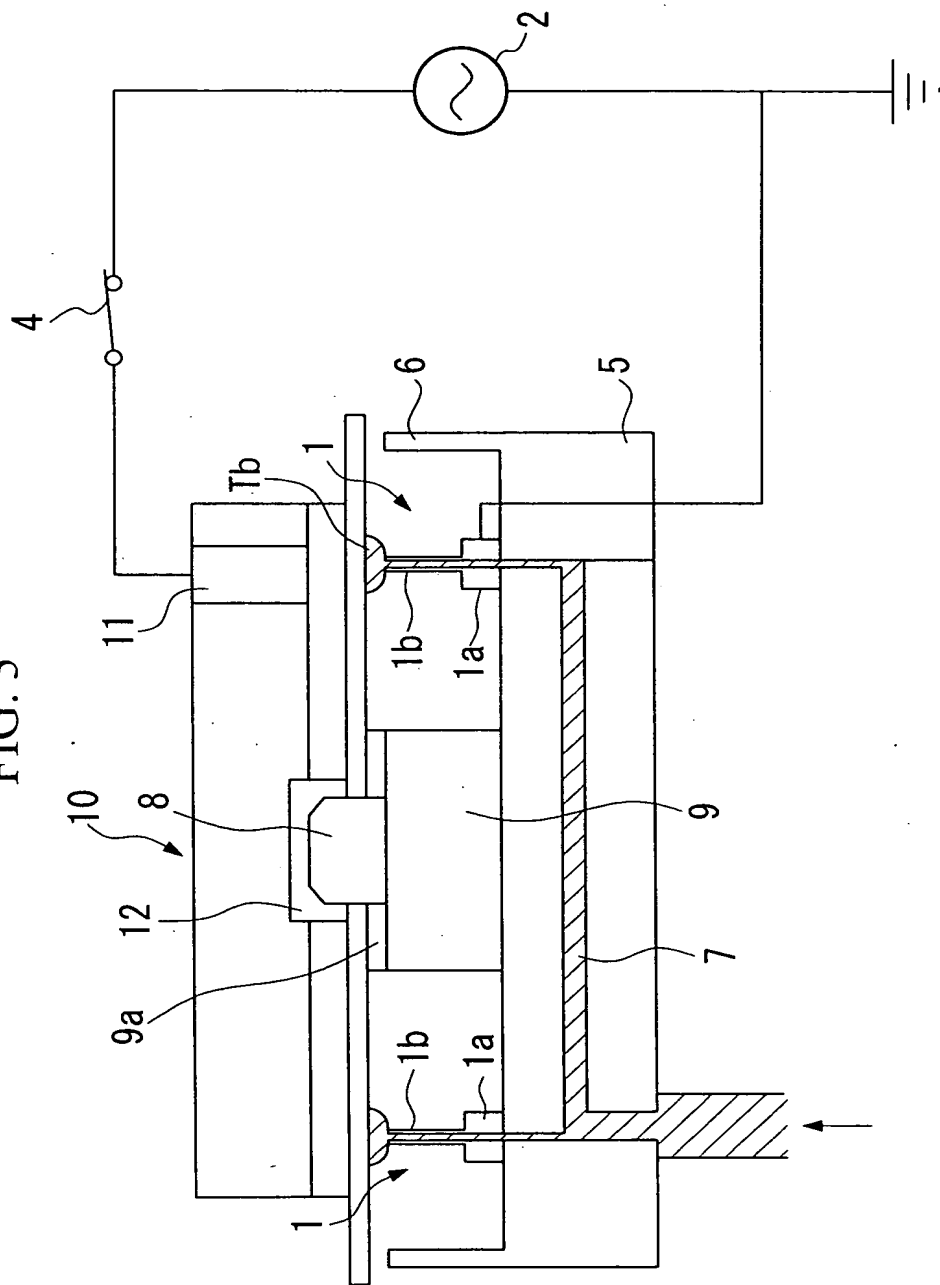


FIG. 3



The diagram illustrates a semiconductor device with two cross-sectional views, A and B. In view A, a substrate 15 contains a central well 21. A top layer 16 is formed on the substrate, with a central protrusion 15A. A gate structure 17 is formed on the top layer, with a central opening 16A. The gate structure 17 is connected to an AC voltage source 18. In view B, the substrate 15 is shown with a central pillar 20. A gate structure 19 is formed on the top layer 16, with a central opening 16A. The gate structure 19 is connected to a DC voltage source. The central pillar 20 is connected to a DC voltage source. The top layer 16 is labeled with 'a' at the edges. The central opening 16A is labeled with 'a' at the edges. The central pillar 20 is labeled with '20A' at the base. The gate structure 17 is labeled with '17' at the base. The AC voltage source 18 is labeled with '18' at the base. The DC voltage source is labeled with '20' at the base.

FIG. 5A

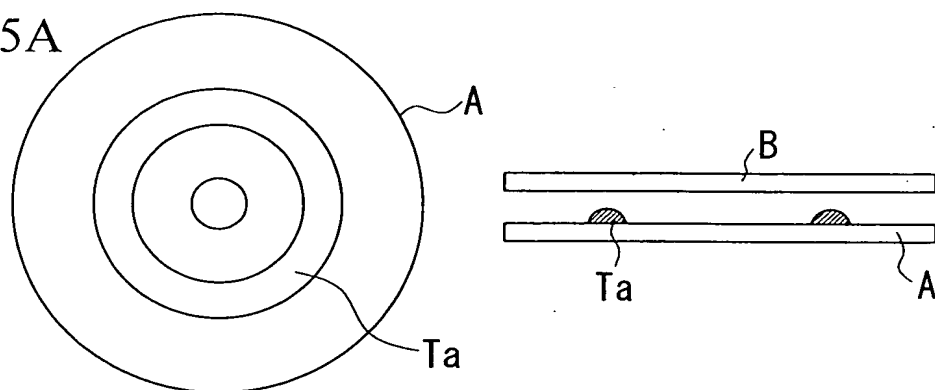


FIG. 5B

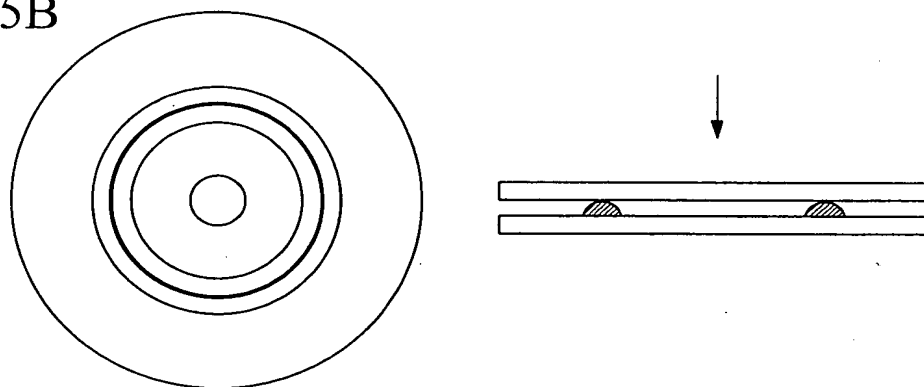


FIG. 5C

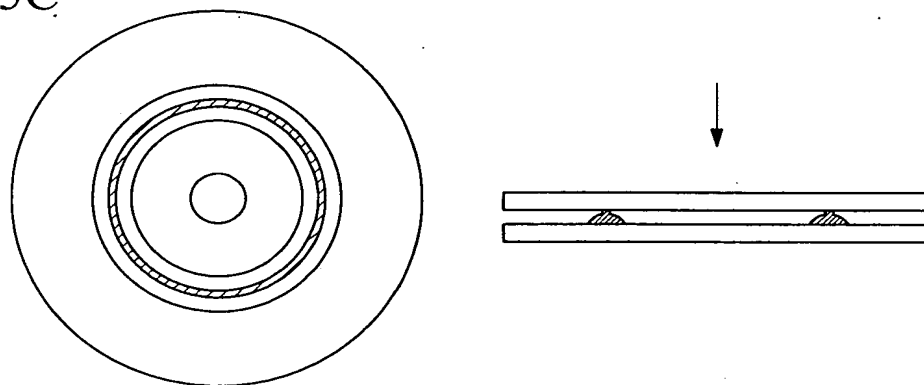


FIG. 5D

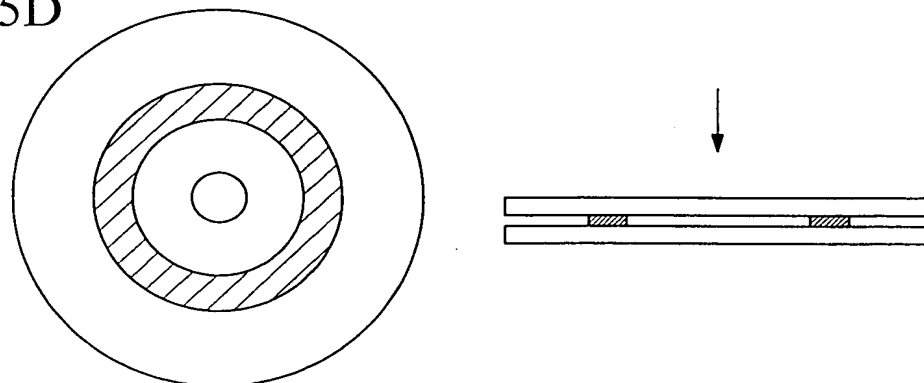


FIG. 6

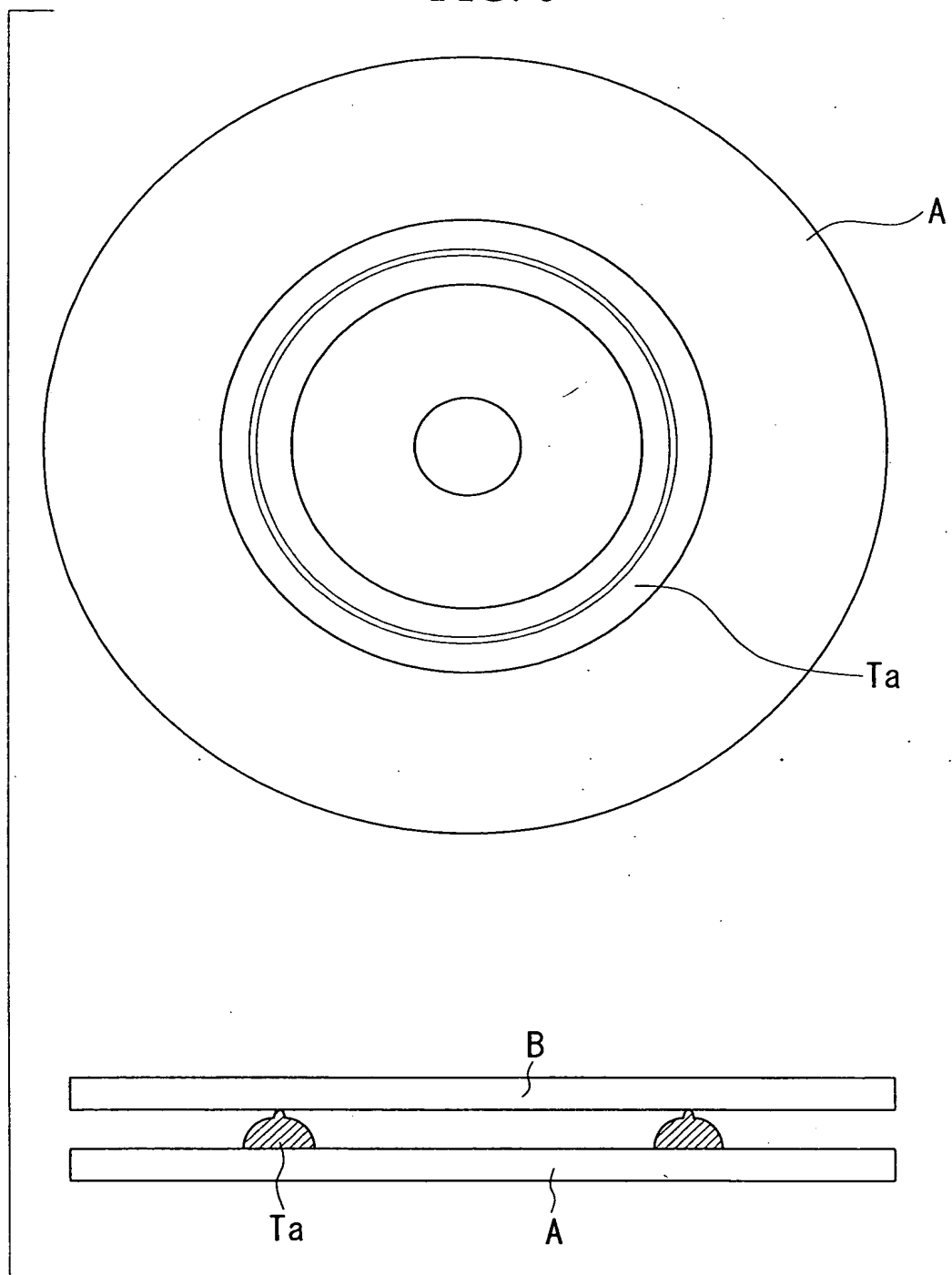


FIG. 7

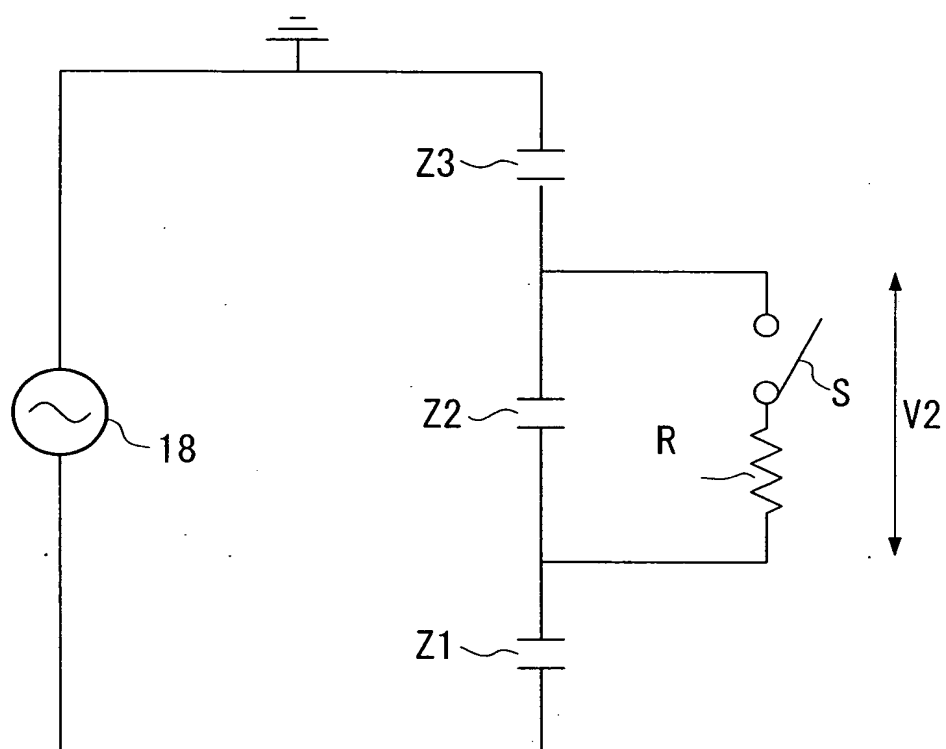


FIG. 8

